WHAT IS CLAIMED IS:

1. A method of forming a thin film transistor, comprising the steps of:

providing an insulating substrate;

forming a polysilicon layer over the substrate;

forming a gate structure over the polysilicon layer, wherein the gate structure includes a gate layer, a gate dielectric layer between the gate layer and the polysilicon layer and a spacer on each sidewall of the gate layer; and

forming a conductive layer over the gate layer and the polysilicon layer.

2. The method of claim 1, wherein the polysilicon layer has a thickness between about 200Å to 500Å.

3. The method of claim 1, wherein the step of forming the conductive layer includes performing a selective deposition according to a selective deposition mechanism due to differences in material properties between the spacer and the polysilicon layer.

4. The method of claim 3, wherein the conductive layer includes an in-situ doped silicon-germanium (SiGe) layer.

5. The method of claim 3, wherein the conductive layer includes a tungsten layer.

6. The method of claim 3, wherein the step of forming the conductive layer includes forming a metal silicide layer by conducting a self-aligned silicide process.

7. The method of claim 3, wherein the step of forming the spacers includes depositing tetra-ethyl-ortho-silicate (TEOS).

8. The method of claim 1, wherein the gate layer includes a polysilicon layer.

9. The method of claim 1, wherein the gate layer includes an in-situ doped polysilicon layer.

10. A method of forming a thin film transistor, comprising the steps of:

providing an insulating substrate;

forming an ultra thin conductive layer over the substrate;

forming a gate structure over the ultra thin conductive layer, wherein the gate structure includes a gate layer, a gate dielectric layer between the gate layer and the ultra thin conductive layer and a spacer on each sidewall of the gate layer; and

forming a conductive layer over the gate layer and the ultra thin conductive layer, wherein a portion of the conductive layer is a source/drain terminal of the thin film transistor.

11. The method of claim 10, wherein the ultra thin conductive layer includes an in-situ doped silicon-germanium (SiGe) layer.

12. The method of claim 10, wherein the ultra thin conductive layer has a thickness between about 200Å to 500Å.

13. The method of claim 10, wherein the step of forming the conductive layer includes performing a selective deposition according to a selective deposition mechanism due to differences in material properties between the spacer and the polysilicon layer.

14. The method of claim 10, wherein the conductive layer includes an in-situ doped silicon-germanium (SiGe) layer.

15. A thin film transistor structure, comprising:

an insulating substrate;

a polysilicon layer over the substrate;

a gate structure over the polysilicon layer, wherein the gate structure includes a gate layer, a gate dielectric layer between the gate layer and the polysilicon layer and a spacer on each side of the gate layer; and

a conductive layer over the gate layer and the polysilicon layer adjacent to the spacers.

16. The structure of claim 15, wherein the polysilicon layer has a thickness between about 250Å to 350Å.

17. The structure of claim 15, wherein the conductive layer includes an in-situ doped silicon-germanium (SiGe) layer.

18. The structure of claim 15, wherein the conductive layer includes a tungsten layer.

19. The structure of claim 15, wherein the conductive layer includes a metal silicide layer.

20. The structure of claim 15, wherein the spacer includes a tetra-ethyl-ortho-silicate (TEOS) layer.